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APPLICATION NUMBER

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FILING OR 371 (c) DATE

FIRST NAMED APPLICANT

ATTORNEY DOCKET NUMBER

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NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given TWO MONTHS from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is unsigned.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of \$65 for a small entity in compliance with 37 CFR 1.27, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is \$65 for a Small Entity

\$65 Late oath or declaration Surcharge.

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- 21. (Previously presented) The MOSFET circuit as claimed in claim 20, wherein the Zener diode and the first resistor are formed by a highly doped polycrystalline layer of a first conduction type and a polycrystalline layer of a second conduction type that is in contact with the highly doped polycrystalline layer.
- 22. (Previously presented) The MOSFET circuit as claimed in claim 21, wherein the polycrystalline layer of the second conduction type is located on a polysilicon gate plane of the MOSFET circuit.
- 23. (Previously presented) The MOSFET circuit as claimed in claim 21, wherein a doping concentration of the highly doped layer is less than 10¹⁹ charge carriers cm⁻³.
- 24. (Currently amended) A MOSFET circuit comprising:
- a first MOS transistor having a first number of cells, the first MOS transistor integrated into a semiconductor body;
- a second MOS transistor having a second number of cells, the second MOS transistor integrated into the semiconductor body, the second number being less than the first number and the second MOS transistor being provided with a source-drain path in parallel with a source-drain path of the first MOS transistor between a voltage source and reference potential, and
- a Zener diode coupled between a gate of the first MOS transistor and a gate of the second MOS transistor, wherein the Zener diode is further coupled between the gate of the second MOS transistor and a control input of the MOSFET circuit, and wherein the Zener diode is forward biased from the control input to the gate of the second MOS transistor.
- 25. (Previously presented) The MOSFET circuit as claimed in claim 24, wherein the first number of cells is at least twice the second number of cells.
- 26. (Previously presented) The MOSFET circuit as claimed in claim 25, wherein the first number of cells is at least ten times the second number of cells.